REMARKS

The application includes claims 1-4, 6-9 and 11-14. In the final Office Action of November 7, 2008, all claims are rejected. With this paper, claims 1, 8 and 12 are amended, none are added and none are canceled.

Claim Rejections under 35 USC §103

Claims 1 and 3-14 are rejected under 35 U.S.C. §103(a) as being unpatentable over Valentaten et al (U.S. Patent 5,250,940, Valentaten hereinafter) in view of Niimura et al (U.S. Publication 2002/0154130 A1, Niimura hereinafter).

Claim 2 is rejected under 35 U.S.C. §103(a) as being unpatentable over Valentaten in view of Niimura and further in view of Leung (U.S Patent 6,760,444).

In the rejected claims, claims 1, 8 and 12 are independent.

With this paper, independent claims 1, 8 and 12 are amended to recite the following features:

> *wherein the memory bus provides the adaptor circuit a plurality of control signal lines for writing or reading data to or from the display device, and a plurality of data signal lines carrying the data,*
>
> *wherein the adaptor circuit provides the display device connection interface a read signal line, a write signal line, an address signal line indicating where on the display device the data should be read or written, and a plurality of data signal lines carrying the data,*
>
> *and wherein the adaptor circuit is configured to convert an update instruction from the processor into an instruction to the display device in a timing order required by the display device for updating only a required part of the display device.*

Support for the amendment can be found in Figures 4, 5 and 6, page 3, lines 10-14, and page 8, lines 17-21 of the originally filed application.

In the Office Action, the adapter circuit of the present application is asserted as being equivalent to the RAM arbiter 18 of Valentaten (page 2, of the Detailed Action). However, it is

respectfully submitted that the functions of the adapter circuit, as defined in the amended claims, are different from that of the RAM arbiter 18 of Valentaten.

According to the present invention as currently claimed, the adapter circuit converts an update instruction from the processor into an instruction to the display device in a timing order required by the display device, and the instruction to the display device updates only a required part of the display device.

Valentaten teaches that the RAM arbiter 18 monitors the address references issued by the embedded processor 14 to identify when the embedded processor 14 seeks access to the RAM 12. Whenever there is no conflict with the embedded processor 14, the video function 16 uses the RAM bus for its own purposes (col. 4, lines 23-29). Valentaten further explains that: "The embedded processor 14 can execute instruction fetch cycles to the ROM 20 while the RAM bus is in use by the video function 16. This allows the embedded processor 14 to keep its instruction queue filled without interfering with the mover and video fetch machine. As stated above, the RAM arbiter 18 can identify the appropriate RAM bus cycles within which to execute video function access to RAM." (Col. 4, lines 30-37)

Thus, the function of the RAM arbiter 18 is, as indicated by its name, to regulate the signal traffic among the embedded processor 14, the RAM 12 and the video circuit 16. As the Office stated in the Response to Arguments, Valentaten discloses that the function of the RAM arbiter 18 is to resolve contention for the memory (i.e. RAM 12) by controlling and prioritize access to the memory (page 5 section 4 of the Detailed Action). It is clear that the RAM arbiter 18 does not have the functionality of "converting an update instruction from the processor into an instruction to the display device in a timing order required by the display device to update only a required part of the display device."

In the Response to Arguments section of the Office Action, the Office mentions other elements that are connected to the RAM arbiter 18 for the claimed functionality, i.e. the video circuit 16 is asserted for generating signals for different monitor screen types, and the embedded processor 14 is asserted for generating data for the video circuit 16. The Office then states that: "Therefore, the system meets the desired balance needed between screen rate and RAM bus utilization." (emphasis added)

Applicant respectfully submits that, the claimed invention, an apparatus comprising a memory bus and an adapter circuit (claim 1), is a functional unit of a system that further comprises a display device and a processor controlling the display device. Of course, the system operates by the processor providing data and instructions to the display device and the display device displaying the data according to the screen type. However, such a system is not the subject of the claimed invention. The claimed invention is a functional unit of the system (see page 2, lines 17-19 of the originally filed application), and the claimed functional unit matches the display device with the controlling processor by converting an update instruction from the controlling processor into an instruction to the display device in a timing order required by the display device for updating only a required part of the display device.

Valentaten does not disclose a circuit that is for connection between a processor and a display device that is configured to convert an update instruction from the controlling processor into an instruction to the display device in a timing order required by the display device for updating only a required part of the display device.

Niimura is merely cited by the Office for disclosing a display device (page 3, lines 2-5 of the Detailed Action). In the system of Niimura as shown in Figure 5, a liquid crystal controller 5 is connected between a processor (CPU 1), UMA memory 3 and a liquid crystal display 9 through an interface FIFO 6. According to Niimura, the liquid crystal controller 5 reads out data from the UMA memory 3, and writes the data in the line driver 7 of the display 9 as indicated by a timing chart 25. In other words, the liquid crystal controller 5 can take in display data collectively for the depth of words of the FIFO, and therefore, chances of dividing memory accesses of the CPU are reduced, and the reduction in the memory band for the CPU can be reduced (paragraph [0036]).

Therefore, the liquid crystal controller of Niimura is not the same as the claimed apparatus. Further, a combination of Valentaten and Niimura does result in an apparatus that is constructed and configured as the claimed invention:

> *wherein the memory bus provides the adaptor circuit a plurality of control signal lines for writing or reading data to or from the display device, and a plurality of data signal lines carrying the data,*
>
> *wherein the adaptor circuit provides the display device connection*

interface a read signal line, a write signal line, an address signal line indicating where on the display device the data should be read or written, and a plurality of data signal lines carrying the data,

and wherein the adaptor circuit is configured to convert an update instruction from the processor into an instruction to the display device in a timing order required by the display device for updating only a required part of the display device.

Based on the foregoing, the amended independent claims 1, 8 and 12 are patentable. In view of the amendment, Applicant respectfully requests the rejections of claims 1, 8 and 12, and all dependent claims thereof, be reconsidered and withdrawn.

Conclusion

It is believed that the application is now in condition for allowance, and early passage to issue is earnestly solicited. The Examiner is invited to contact applicant's attorney at the number below if there are any questions.

Respectfully submitted,

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